

Exhibit 8



U.S. Patent No. 8,193,792 (“’792 Patent”)

Accused Products

Samsung products with Intel processors featuring Fully Integrated Voltage Regulators, including without limitation the Samsung Galaxy Book Flex 13.3” NP930QCG-K01US (“Accused Products”), infringe at least Claims 1 and 10 of the ’792 Patent.

Claim 1

Claim 1	Accused Products
[1pre] A circuit comprising:	<p>To the extent the preamble is limiting, each Accused Product comprises the claimed circuit.</p> <p>For example, the Galaxy Book Flex includes a 10th-generation Intel Core processor, which contains Intel Fully Integrated Voltage Regulator technology.</p> <p><i>See, e.g.:</i></p> <div data-bbox="634 703 1356 935"><p>Processor Processor / Chipset Intel® Core™ i7-1065G7 Processor</p></div> <p>Screenshot identifying Intel Core i7-1065G7 processor from https://www.samsung.com/us/computing/galaxy-books/galaxy-book-flex/galaxy-book-flex-13-3-qlcd-512gb-storage-s-pen-included-np930qcg-k01us/</p>

Claim 1	Accused Products				
	<div data-bbox="636 272 1892 1040"><div data-bbox="636 272 1892 589"><div data-bbox="804 272 1472 315">Intel® Core™ i7-1065G7 Processor</div><div data-bbox="804 337 1146 373">8M Cache, up to 3.90 GHz</div><div data-bbox="1119 406 1404 459"><input type="checkbox"/> Add to Compare</div><div data-bbox="1167 493 1354 526">Find a System</div></div><div data-bbox="653 612 858 647">Specifications</div><div data-bbox="661 670 924 706"> Export specifications</div><div data-bbox="661 714 806 745">Essentials</div><div data-bbox="661 774 1858 906"><table><tr><td>Product Collection</td><td>10th Generation Intel® Core™ i7 Processors</td></tr><tr><td>Code Name</td><td>Products formerly Ice Lake</td></tr></table></div><div data-bbox="636 927 1858 1036"><p>Screenshot identifying Intel Core i7-1065G7 as a 10th Generation Core processor (formerly Ice Lake) from https://ark.intel.com/content/www/us/en/ark/products/196597/intel-core-i7-1065g7-processor-8m-cache-up-to-3-90-ghz.html</p></div></div>	Product Collection	10th Generation Intel® Core™ i7 Processors	Code Name	Products formerly Ice Lake
Product Collection	10th Generation Intel® Core™ i7 Processors				
Code Name	Products formerly Ice Lake				

Claim 1	Accused Products
	<p style="text-align: right;">Circuit</p> <p>Figure 1-1. U-Processor Line and Y-Processor Line Platforms</p> <p>Screenshot, with annotation illustrating the claimed circuit, from https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html</p>
[1a] a first voltage regulator;	<p>Each Accused Product includes a first voltage regulator.</p> <p>For example, the Galaxy Book Flex includes an Intel 10th-generation Core processor featuring Intel's Fully Integrated Voltage Regulator ("FIVR") technology, including a first voltage regulator that provides a supply voltage to the circuit section at a voltage and current level suitable for use by the processor's information processing features ("cores") during operating mode, as explained more fully below.</p> <p><i>See, e.g.:</i></p>

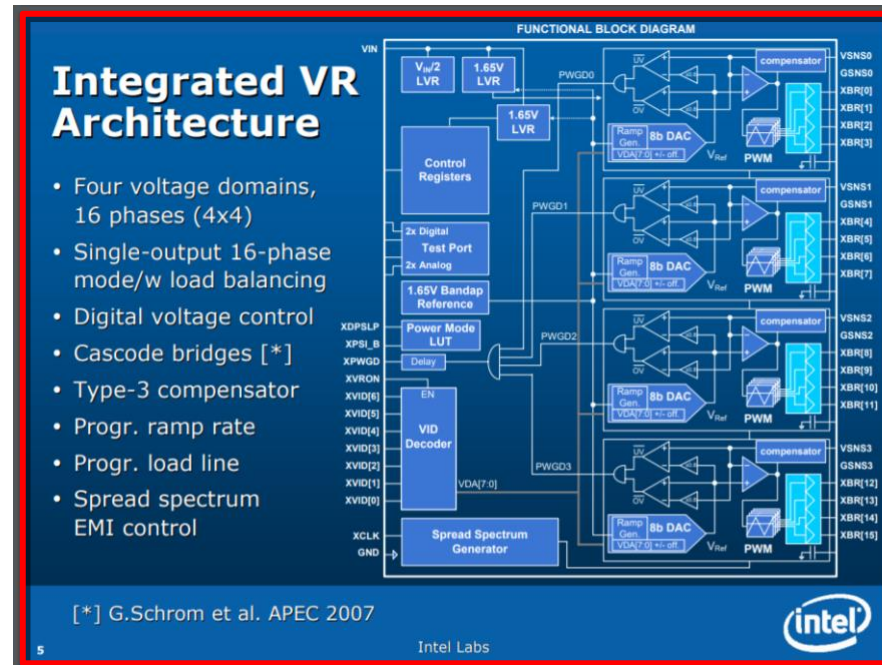
Claim 1	Accused Products
	<p data-bbox="659 280 1356 318">12.1.2 Integrated Voltage Regulator</p> <p data-bbox="827 342 1864 428">Due to the integration of platform voltage regulators into the processor, the processor has one main voltage rail (V_{CCIN}), the PCH has one main voltage rail (V_{CCIN_AUX}) and a voltage rail for the memory interface (V_{DDQ}).</p> <p data-bbox="827 428 1835 574">The voltage rail V_{CCIN} will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the Cores, cache, System Agent, TCSS and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The V_{CCIN} rail will remain a VID-based voltage with a loadline similar to the core voltage rail in previous processors.</p> <p data-bbox="632 613 1814 716">Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, <i>available at</i> https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</p>

Plurality of voltage regulators (FIVR)

Claim 1

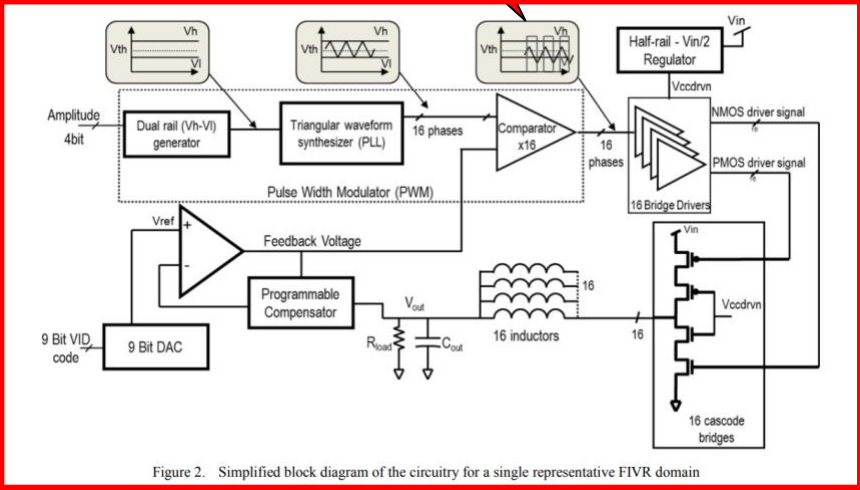
Accused Products

Plurality of voltage regulators (FIVR)



Screenshot, with annotation illustrating the plurality of voltage regulators within the Intel processor, of which one is the first voltage regulator, from <https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf>

Claim 1	Accused Products
	<div data-bbox="630 259 1060 909"> <h3>Haswell Platform</h3> <p>The diagram illustrates the Haswell Platform architecture. It features a central Haswell Processor block. To the left of the processor, there are two green boxes representing voltage regulators: 'Vcc_In VR 0V-1.8V' and 'DDR VR'. Arrows indicate connections from these regulators to the processor. The processor itself is divided into two main sections: 'FIVR VRs' and 'Logic'. The 'FIVR VRs' section lists various functional blocks: System, I/O, Analog, Core 0, Core 1, Core 2, Core 3, Cache, Graphics0, Graphics1, EDRAM, and OPIO. The 'Logic' section is also listed. A red callout box with a pointer identifies the 'System I/O' as the 'First voltage regulator'.</p> </div> <p>Screenshot, with annotation, from https://www.pdma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-voltage-regulator.pdf</p>

Claim 1	Accused Products
	<p data-bbox="919 261 1150 391" style="background-color: red; color: black; text-align: center;">FIVR circuit architecture (1st and 2nd Voltage regulator)</p>  <p data-bbox="789 927 1335 943">Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain</p> <p data-bbox="638 959 1864 1024">Screenshot, with annotation, from https://www.researchgate.net/publication/271416878_FIVR - Fully integrated voltage regulators on 4th generation IntelR Core SoCs</p>
[1b] a second voltage regulator; and	<p data-bbox="638 1057 1388 1089">Each Accused Product includes a second voltage regulator.</p> <p data-bbox="638 1114 1843 1292">For example, the Galaxy Book Flex includes an Intel 10th-generation Core processor featuring Intel's Fully Integrated Voltage Regulator ("FIVR") technology, including a second voltage regulator that provides a standby voltage to the circuit section at a voltage and current level suitable for use by the processor's memory element ("cache") during sleep mode, as explained more fully below.</p> <p data-bbox="638 1317 751 1349"><i>See, e.g.:</i></p>

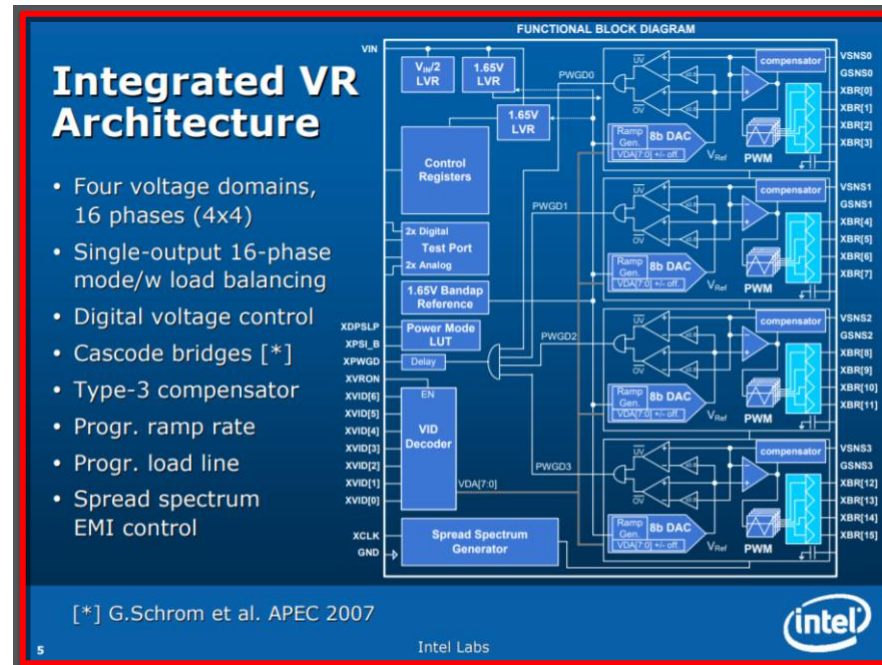
Claim 1	Accused Products
	<p>12.1.2 Integrated Voltage Regulator</p> <p>Due to the integration of platform voltage regulators into the processor, the processor has one main voltage rail (V_{CCIN}), the PCH has one main voltage rail (V_{CCIN_AUX}) and a voltage rail for the memory interface (V_{DDQ}).</p> <p>The voltage rail V_{CCIN} will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the Cores, cache, System Agent, TCSS and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The V_{CCIN} rail will remain a VID-based voltage with a loadline similar to the core voltage rail in previous processors.</p> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, <i>available at</i> https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</p>

Plurality of voltage regulators (FIVR)

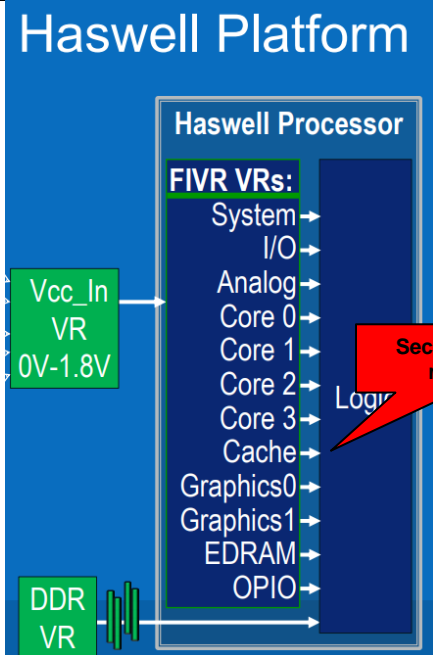
Claim 1

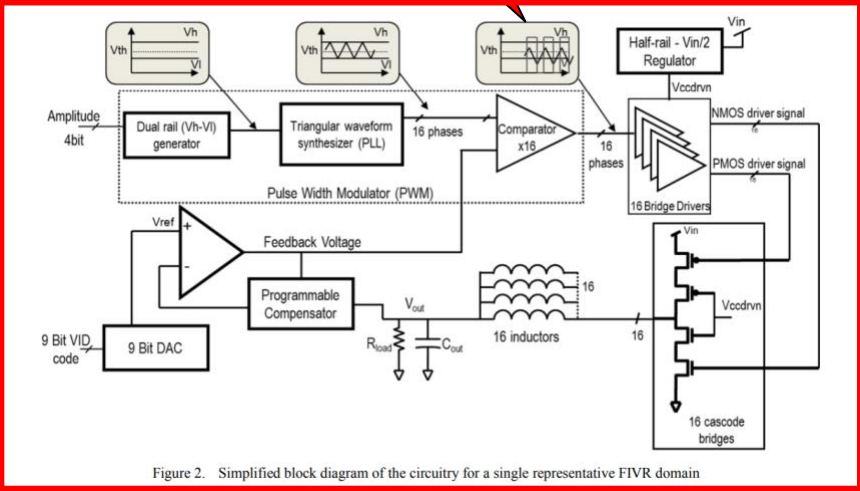
Accused Products

Plurality of voltage regulators (FIVR)

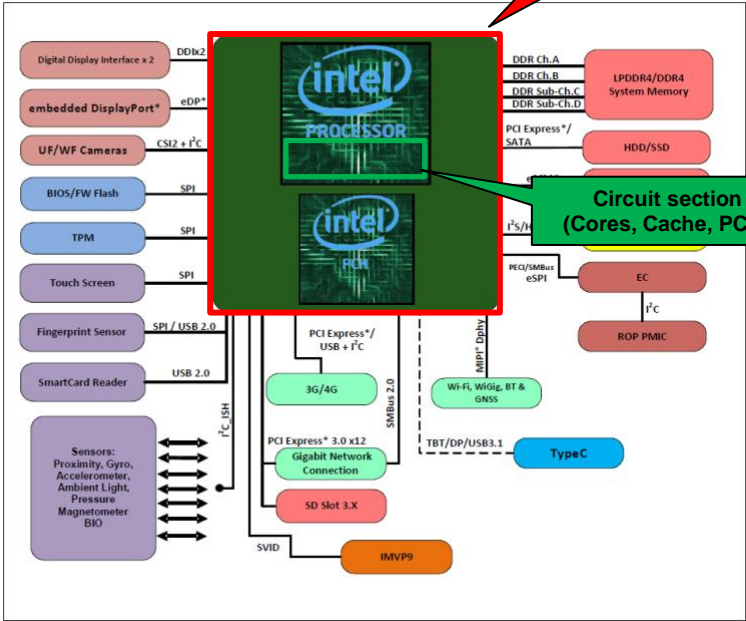


Screenshot, with annotation illustrating the plurality of voltage regulators within the Intel processor, of which one is the second voltage regulator, from <https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf>



Claim 1	Accused Products
	<div data-bbox="630 259 1060 909"> <h3>Haswell Platform</h3>  <p>Haswell Processor</p> <p>FIVR VRs:</p> <ul style="list-style-type: none"> System → I/O → Analog → Core 0 → Core 1 → Core 2 → Core 3 → Cache → Graphics0 → Graphics1 → EDRAM → OPIO → <p>Vcc_In VR 0V-1.8V</p> <p>DDR VR</p> <p>Second voltage regulator</p> </div> <p>Screenshot, with annotation, from https://www.pdma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-voltage-regulator.pdf</p>

Claim 1	Accused Products
	<p data-bbox="919 261 1150 391">FIVR circuit architecture (1st and 2nd Voltage regulator)</p>  <p data-bbox="789 927 1335 943">Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain</p> <p data-bbox="638 959 1864 1024">Screenshot, with annotation, from https://www.researchgate.net/publication/271416878_FIVR - Fully integrated voltage regulators on 4th generation IntelR Core SoCs</p>
[1c] a circuit section, the circuit section comprising a memory element and operable to:	<p data-bbox="638 1057 1892 1089">Each Accused Product includes a circuit section, the circuit section comprising a memory element.</p> <p data-bbox="638 1114 1864 1219">For example, the Galaxy Book Flex includes an Intel 10th-generation Core processor featuring a Last Level Cache (“LLC”). The claimed circuit section comprises the LLC, the processor’s information processing unit (cores), and the power control unit.</p> <p data-bbox="638 1243 747 1276"><i>See, e.g.:</i></p>

Claim 1	Accused Products
	<p>2.4.1 Intel® Smart Cache Technology</p> <p>The Intel® Smart Cache Technology is a shared Last Level Cache (LLC).</p> <ul style="list-style-type: none"> • The LLC may also be referred to as a third level cache. • The LLC is shared between all IA cores as well as the Processor Graphics. • The first and second level caches are not shared between physical cores and each physical core has a separate set of caches. • The size of the LLC is SKU specific with a maximum of 2 MB per physical core and is a 16 way associative cache. <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, <i>available at</i> https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</p>

Claim 1	Accused Products
	<p data-bbox="1270 259 1537 305">Circuit</p> <p data-bbox="640 321 1228 344">Figure 1-1. U-Processor Line and Y-Processor Line Platforms</p>  <p data-bbox="634 977 1879 1079">Annotated screenshot showing circuit and circuit section from https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html.</p>
<p data-bbox="205 1112 598 1214">[1d] receive a supply voltage from the first voltage regulator when in an operating mode;</p>	<p data-bbox="634 1112 1879 1177">In each Accused Product, the circuit section is operable to receive a supply voltage from the first voltage regulator when in an operating mode.</p> <p data-bbox="634 1205 1879 1307">For example, the Galaxy Book Flex receives a certain core voltage from the first voltage regulator while in an operating mode, such as a C0 state (“The normal operating state of a processor IA core where code is being executed”).</p> <p data-bbox="634 1334 745 1367"><i>See, e.g.:</i></p>

Claim 1	Accused Products						
	<div>operating mode</div> <p>Table 3-4. Core C-states</p> <table><tr><th>Core C-State</th><th>C-State Request Instruction</th><th>Description</th></tr><tr><td>C0</td><td>N/A</td><td>The normal operating state of a processor IA core where code is being executed</td></tr></table> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, <i>available at</i> https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</p>	Core C-State	C-State Request Instruction	Description	C0	N/A	The normal operating state of a processor IA core where code is being executed
Core C-State	C-State Request Instruction	Description					
C0	N/A	The normal operating state of a processor IA core where code is being executed					

Claim 1	Accused Products
	<p>Software Impact to Platform Energy</p> <p>Operating mode (first voltage regulator on)</p>  <p>Figure 4: Flexible C-state Select Idle Power Level vs. Responsiveness</p>  <p>Annotated screenshot from https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf</p>
<p>[1e] transition from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section; and</p>	<p>In each Accused Product, the circuit section is operable to transition from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section.</p> <p>For example, the Intel processor in the Galaxy Book Flex can transition into a sleep mode, such as the C6 state, in which the information processor units flush their L1 instruction/data caches and L2 caches, save their architectural state, deactivate their inputs, and deactivate the first voltage regulator.</p>

Claim 1

Accused Products

See, e.g.:

Table 3-4. Core C-states

Core C-State	C-State Request Instruction	Description
C0	N/A	The normal executed state. Core is being
C1	MWAIT(C1)	AutoHalt - Core execution stopped, waiting for package in C0 state
C1E	MWAIT(C1E)	Core C1 + lowest frequency and voltage state
C6-C10	MWAIT(C6/7/7s/ C8/9/10) or IO read=P_LVL3/4/5/6/7/8	Processor IA, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache cores save their architectural state to a SRAM before reducing IA cores voltage, if possible may also be reduced to 0V. Core clocks are off.

Sleep mode

deactivation of inputs

Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, available at <https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf>

Software Impact to Platform En

Sleep mode
(Core IVR off)

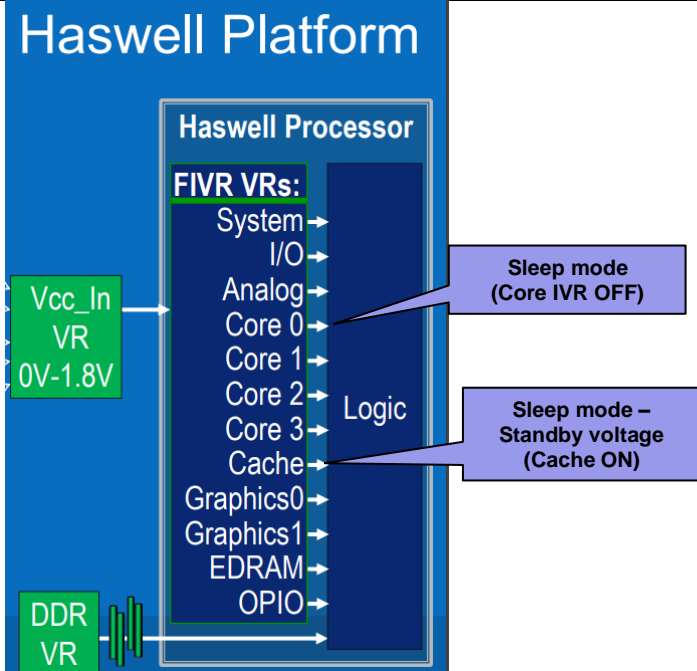


Figure 4: Flexible C-states to select Idle Level vs. Responsiveness



Illustrated screenshot from <https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf>

Claim 1	Accused Products																																																															
<p>[1f] receive a standby voltage from the second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in the memory element.</p>	<p>In each Accused Product, the circuit section is operable to receive a standby voltage from the second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in the memory element.</p> <p>For example, the Intel processor in the Galaxy Book Flex continues to operate the integrated voltage regulator associated with the Last Level Cache during sleep mode (such as the C6 core state) in order to receive a lower voltage sufficient to preserve the contents of the LLC memory.</p> <p>See, e.g.</p> <div><p>Software Impact to Platform Energy-Efficiency</p><p>Core receives supply voltage during operating mode</p><p>Figure 4: Flexible C-states to Power Level vs. Responsiveness</p><table><thead><tr><th>Active state</th><th>C0</th><th>C1</th><th>C3</th><th>C6/C7</th><th>PC7 Transition</th><th>PC7</th></tr></thead><tbody><tr><td>Core voltage*</td><td>High</td><td>High</td><td>High</td><td>Low</td><td>Low</td><td>Low</td></tr><tr><td>Core clock</td><td>On</td><td>off</td><td>off</td><td>off</td><td>off</td><td>off</td></tr><tr><td>PLL</td><td>On</td><td>On</td><td>off</td><td>off</td><td>off</td><td>off</td></tr><tr><td>L1/L2 caches</td><td>On</td><td>On</td><td>On</td><td>On</td><td>On</td><td>On</td></tr><tr><td>LLC/L3 cache</td><td>On</td><td>On</td><td>On</td><td>On</td><td>On</td><td>On</td></tr><tr><td>Wakeup time*</td><td>Active</td><td>Fast</td><td>Fast</td><td>Fast</td><td>Fast</td><td>Slow</td></tr><tr><td>Idle power*</td><td>Active</td><td>Low</td><td>Low</td><td>Low</td><td>Low</td><td>Low</td></tr><tr><td>Transition energy*</td><td>Active</td><td>Low</td><td>Low</td><td>Low</td><td>Low</td><td>Low</td></tr></tbody></table><p>* Rough approximation</p><p>LLC receives lower voltage from its IVR during sleep</p></div>	Active state	C0	C1	C3	C6/C7	PC7 Transition	PC7	Core voltage*	High	High	High	Low	Low	Low	Core clock	On	off	off	off	off	off	PLL	On	On	off	off	off	off	L1/L2 caches	On	On	On	On	On	On	LLC/L3 cache	On	On	On	On	On	On	Wakeup time*	Active	Fast	Fast	Fast	Fast	Slow	Idle power*	Active	Low	Low	Low	Low	Low	Transition energy*	Active	Low	Low	Low	Low	Low
Active state	C0	C1	C3	C6/C7	PC7 Transition	PC7																																																										
Core voltage*	High	High	High	Low	Low	Low																																																										
Core clock	On	off	off	off	off	off																																																										
PLL	On	On	off	off	off	off																																																										
L1/L2 caches	On	On	On	On	On	On																																																										
LLC/L3 cache	On	On	On	On	On	On																																																										
Wakeup time*	Active	Fast	Fast	Fast	Fast	Slow																																																										
Idle power*	Active	Low	Low	Low	Low	Low																																																										
Transition energy*	Active	Low	Low	Low	Low	Low																																																										
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Claim 1	Accused Products
	 <p>Haswell Platform</p> <p>Haswell Processor</p> <p>FIVR VRs:</p> <ul style="list-style-type: none"> System I/O Analog Core 0 Core 1 Core 2 Core 3 Cache Graphics0 Graphics1 EDRAM OPIO <p>Logic</p> <p>Vcc_In VR 0V-1.8V</p> <p>DDR VR</p> <p>Sleep mode (Core IVR OFF)</p> <p>Sleep mode - Standby voltage (Cache ON)</p> <p>Illustrated screenshot from https://www.pdma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf</p>

Claim 10

Claim 10	Accused Products
[10pre] A method comprising:	To the extent the preamble is limiting, each Accused Product performs the claimed method. <i>See supra</i> claim element [1pre].
[10a] delivering to a circuit section of a circuit a supply voltage from a first voltage	Each Accused Product performs delivering to a circuit section of a circuit a supply voltage from a first voltage regulator when in an operating mode.

Claim 10	Accused Products
regulator when in an operating mode;	<i>See supra</i> claim element [1d].
[10b] transitioning from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section; and	Each Accused Product performs transitioning from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section. <i>See supra</i> claim element [1e].
[10c] delivering to the circuit section a standby voltage from a second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in a memory element.	Each Accused Product performs delivering to the circuit section a standby voltage from a second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in a memory element. <i>See supra</i> claim element [1f].